

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES LETTERS PATENT

Title:

BOOSTING VOLTAGE CONTROL CIRCUIT

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BOOSTING VOLTAGE CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

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Field of the Invention

The present invention relates to a boosting voltage control circuit, and more particularly, to a boosting voltage control circuit capable of supplying a constant voltage to word lines upon a read operation in the flash memory.

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Background of the Related Art

In a flash memory device of a low power supply voltage, voltage boosting is performed in order to boost a word line gate voltage of the cell every time the read operation of the cell is performed. In other words, boosting is to boost a low power supply voltage (VCC) to a voltage level that could be used for the read operation. Generally, the boosting operation raises a voltage of 0V to 5.3V if a read command is inputted from the outside. However, in raising the voltage from 0V to 5.3V, lots of time is taken due to various delay components such as a RC delay, etc. within the boosting circuit.

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SUMMARY OF THE INVENTION

Accordingly, the present invention is contrived to substantially obviate one or more problems due to limitations and disadvantages of the related art, and an object of the present invention is to provide a boosting voltage control

circuit capable of improving the speed of a read operation and minimizing the current flowing in a standby state, by keeping a voltage of a constant level in the standby state as well as the read operation

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a boosting voltage control circuit according to the present invention is characterized in that it comprises, in order to constantly keep a level of a voltage boosted by a pump, a boosting voltage dividing means for dropping a boosting voltage, a package voltage generating means for generating package voltage signals of various voltage levels depending on external trim bits, a compare reference voltage generating means for generating a reference voltage and a control voltage according to the package voltage signal from the package voltage generating means, a compare means driven by a control voltage, for comparing the dropped boosting voltage and the reference voltage to output a compare result signal, an output means for outputting first and second clock control signals using the compare result signal from the compare means, a clock generator for generating clock signals according to the first and second

clock control signals, and a first pump for always outputting the boosting voltage according to the clock signal and a second pump for outputting the boosting voltage according to an external read signal and the clock signal.

Further, a boosting voltage control circuit having a pump for
5 transferring a pumped voltage, as an output, according to the output signal of a clock generator, and a regulation block for detecting a voltage of the output to control the clock generator according to the present invention is characterized in that the regulation block comprises a boosting voltage dividing means for dropping a voltage of the output to a given level, a package voltage generating
10 means for generating package voltage signals of various voltage levels according to external trim bits, a compare reference voltage generating means for generating a reference voltage and a control voltage according to the package voltage signal, and a compare means for comparing the output of the voltage dividing means and the reference voltage according to the control
15 voltage to generate a control signal for controlling the clock generator.

In another aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

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BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following detailed description of the preferred embodiments of the invention in conjunction with the accompanying

drawings, in which:

FIG. 1 is a block diagram of a boosting voltage control circuit according to the present invention for explaining the entire structure and operation of the circuit,

5 FIG. 2 is a circuit diagram of a regulation block according to the present invention for explaining the construction and operation of the block,

FIG. 3A ~ FIG. 3C are circuit diagrams of a package voltage generating unit according to the present invention for explaining the construction and operation of the unit, and

10 FIG. 4 is a circuit diagram of a clock generator according to the present invention for explaining the construction and operation of the generator.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the preferred embodiments of
15 the present invention, examples of which are illustrated in the accompanying drawings, in which like reference numerals are used to identify the same or similar parts. FIG. 1 is a block diagram of a boosting voltage control circuit according to the present invention for explaining the entire structure and operation of the circuit.

20 Referring to FIG. 1, a regulation block **100** is coupled between a boosting voltage output **OBvt** and a clock generator **200**. First and second pumps **300** and **310** are connected in parallel between the clock generator **200** and the boosting voltage output **OBvt**. The first pump **300** is driven by an external read enable signal **ERead**.

An operation of the voltage regulation circuit constructed above will be below described.

The second pump **310** generates a boosting voltage **BOOST** of a constant level according to clock signals **CLK<0:4>** of the clock generator **200** in a standby state as well as a read state. The first pump **300** generates the boosting voltage **BOOST** of a constant level according to the external read enable signal **ERead** and the clock signals **CLK<0:4>** of the clock generator **200**. The regulation block **100** compares the boosting voltage **BOOST** with the reference voltage generated by an internal trim bit and then outputs first and second clock control signals **PBIAS** and **NBIAS** for keeping the boosting voltage **BOOST** outputted from the first and second pumps **300** and **310** to be a constant level. The clock generator **200** controls the first and second pumps **300** and **310** by changing the period of the clock signals **CLK<0:4>** depending on the first and second clock control signals **PBIAS** and **NBIAS**.

In the present invention, while the regulation block **100** senses the boosting voltage **BOOST** at the output terminal as an output feedback mode, if any abnormality occurs in the boosting voltage **BOOST**, the regulation block **100** controls the clock signal **CLK** being the output of the clock generator **200** using the first and second clock control signals **PBIAS** and **NBIAS** being the output of the regulation block **100**, thereby controlling the first and second pumps **300** and **310** to control the outputted boosting voltage **BOOST**.

The first pump **300** is a first boosting means for boosting the word line gate voltage when the read operation of the device is performed. The second pump **310** is a second boosting means for generating the boosting voltage

normally in order to shorten time taken to boost the word line gate voltage. As more current is consumed during the read state rather than the standby state, the first and second pumps **300** and **310** are positioned. In other words, in the standby state, only the second pump **310** operates to generate a low current and a boosting voltage of a constant level. If a read command is inputted, the first and second pumps **300** and **310** operate to supply a high current and a boosting voltage of a constant level. Thereby, it is possible to reduce the read time of the device and the power consumption of the standby state.

The regulation block **100** for comparing the levels of the boosting voltages **BOOST** to output the first and second clock control signals **PBIAS** and **NBIAS** will be now described.

FIG. 2 is a circuit diagram of a regulation block according to the present invention for explaining the construction and operation of the block.

Referring to FIG. 2, the regulation block **100** comprises a boosting voltage dividing unit **110**, a compare unit **120**, a reference voltage generating unit **130**, a clock control signal output unit **140** and a package voltage generating unit **150**. The input of the boosting voltage dividing unit **110** is connected to the boosting voltage output **OBvt** in FIG. 1 and its output is connected to a first compare signal **VBDIV** input of the compare unit **120**. The input of the reference voltage generating unit **130** is connected to the output of the package voltage generating unit **150**. First and second outputs of the reference voltage generating unit **130** are connected to a second compare signal **REFCRV** input and a control signal **NGATE** input of the compare unit **120**, respectively. The output of the compare unit **120** is

connected to the input of the clock control signal output unit **140**. The input of the clock control signal output unit **140** is connected to the output of the compare unit **120**. First and second outputs of the clock control signal output unit **140** is connected to the input of the clock generator **200**. First and third
5 inputs of the package voltage generating unit **150** are connected to external trim bits **TE1** through **TE3**, respectively, and the output of the package voltage generating unit **150** is connected to the input of the reference voltage generating unit **130**.

The operation and construction of the regulation block having the above
10 connection relationship will be described in detail by reference to FIG. 3. A term ‘diode-connected transistor’ to be described in the later means that a transistor in which one of the gate terminal, the source terminal and the drain terminal is connected operates as a diode.

The boosting voltage dividing unit **110** comprises tenth ~ fifteenth
15 PMOS transistors **P10** through **P15** which are diode-connected. In concrete, each of the tenth ~ fifteenth PMOS transistors **P10** through **P15** gate terminals of which are connected to the source terminals thereof is sequentially serially connected between the boosting voltage input terminal **OBvt** and the ground **VSS**. In other words, the drain terminal of the tenth PMOS transistor
20 **P10** is connected to the boosting voltage input terminal **OBvt**. The source terminal of the tenth PMOS transistor **P10** is connected to the drain terminal of the eleventh PMOS transistor **P11**. The source terminal of the eleventh PMOS transistor **P11** is connected to the drain terminal of the twelfth PMOS transistor **P12**. The source terminal of the twelfth PMOS transistor **P12** is

connected to the drain terminal of the thirteenth PMOS transistor **P13**. The source terminal of the thirteenth PMOS transistor **P13** is connected to the drain terminal of the fourteenth PMOS transistor **P14**. The source terminal of the fourteenth PMOS transistor **P14** is connected to a tenth node **Q10**. The drain terminal of the fifteenth PMOS transistor **P15** is also connected to the tenth node **Q10**. The source terminal of the fifteenth PMOS transistor **P15** is connected to the ground **VSS**.

The reference voltage generating unit **130** comprises tenth and eleventh NMOS transistors **N10** and **N11** which are diode-connected to a sixteenth PMOS transistor **P16**. In concrete, the sixteenth PMOS transistor **P16** driven by a package voltage **PVT** being the output of the package voltage generating unit **150** is connected between the power supply voltage **VCC** and an eleventh node **Q11**. The tenth NMOS transistor **N10** drain and gate terminals of which are connected is connected between the eleventh node **Q11** and a twelfth node **Q12**. The eleventh NMOS transistor **N11** drain and gate terminals of which are connected is connected between the twelfth node **Q12** and the ground **VSS**.

The compare unit **120** comprises a differential amplifier having seventeenth and eighteenth PMOS transistors **P17** and **P18** and twelfth ~ thirteenth NMOS transistors **N12** and **N13**, and a fourteenth NMOS transistor **N14** for driving the differential amplifier. In concrete, the seventeenth PMOS transistor **P17** is connected to the power supply voltage **VCC** and a thirteenth node **Q13** and is driven by the potential of the thirteenth node **Q13**. The eighteenth PMOS transistor **P18** is connected to the power supply voltage

VCC and a fourteenth node **Q14** and is driven by the potential of the thirteenth node **Q13**. The twelfth NMOS transistor **N12** is connected between the thirteenth node **Q13** and the fifteenth node **Q15**, and is driven by the tenth node **Q10** (output of the boosting voltage dividing means; **VBDIV**). The
5 thirteenth NMOS transistor **N13** is connected between the fourteenth node **Q14** and the fifteenth node **Q15**, and is driven by an eleventh node **Q11** (output of the compare reference voltage generating means; **REFCRV**). The fourteenth NMOS transistor **N14** is connected between the fifteenth node **Q15** and the ground **VSS** and is driven by the potential of a twelfth node **Q12**.

10 The clock control signal output unit **140** comprises a nineteenth PMOS transistor **P19** and a fifteenth NMOS transistor **N15**. The nineteenth PMOS transistor **P19** and the fifteenth NMOS transistor **N15**, which are diode-connected, are connected between the power supply voltage **VCC** and the ground **VSS**. In concrete, the nineteenth PMOS transistor **P19** the gate
15 terminal of which is connected to the source terminal thereof is connected to the power supply voltage **VCC** and the output terminal of the second clock control signal **NBIAS**. The fifteenth NMOS transistor **N15** is connected between the output terminal of the first clock control signal **PBIAS** and the ground terminal **VSS**, and is driven by the potential of the fourteenth node
20 **Q14**.

The operation of the regulation block constructed above will be below described.

The boosting voltage dividing unit **110** drops the boosting voltage **BOOST** inputted through the tenth ~ fifteenth PMOS transistors **P10** through

P15 which are diode-connected. The unit **110n** outputs the first compare signal **VBDIV** being the boosting voltage, which was dropped, to the first compare signal **VBDIV** input terminal of the compare unit **120**. For example, if the boosting voltage **BOOST** is 9V, the voltage applied to both ends of each of the tenth ~ fifteenth PMOS transistors **P10** through **P15** becomes 1.5V. The voltage applied to both end of the fifteenth PMOS transistor **P15** becomes a voltage that the boosting voltage **BOOST** is divided equally by 6, i.e., 1.5V.

The reference voltage generating unit **130** divides the power supply voltage **VCC** through the sixteenth PMOS transistor **P16**, and the tenth and eleventh NMOS transistors **N10** and **N11** to generate the second compare signal **REFCRV** for comparing the level of the boosting voltage and the control signal **NGATE** for controlling the operation of the compare unit **120**. In concrete, the voltage applied to both ends of the sixteenth PMOS transistor **P16** is changed by the package voltage **PVT** being the output of the package voltage generating unit **150**. Thereby, the voltage levels of the second compare signal **REFCRV** being the output of the reference voltage generating unit **130** and the control signal **NGATE** are changed. This is because as the channel width of the sixteenth first6 PMOS transistor **P16** is adjusted according to the package voltage signal **PVT**, the voltage applied to the sixteenth PMOS transistor **P16** is changed. The remaining voltage subtracted from the voltage applied to both ends of the sixteenth PMOS transistor **P16** in the power supply voltage is divided into two parts by the tenth and eleventh NMOS transistors **N10** and **N11**. Thereby, the voltage of the eleventh and twelfth nodes **Q11** and **Q12** is adjusted by controlling the voltage applied to

both ends of the sixteenth PMOS transistor **P16**. For example, assuming that the power supply voltage **VCC** is 5V and the voltage applied to the sixteenth PMOS transistor **P16** is 1V by the package voltage signal **PVT**, 2V is applied to the eleventh node **Q11** and the twelfth node **Q12**, respectively, by means of the tenth and eleventh NMOS transistors **N10** and **N11**.

The compare unit **120** generates a compare result signal being the output of the compare unit **120** according to the first compare signal **VBDIV** being the output of the boosting voltage dividing unit **110** and the second compare signal **REFCRV** being the output of the reference voltage generating unit **130**.

In more detail, the fourteenth NMOS transistor **N14** is turned on by the control signal **NGATE** of the reference voltage generating unit **130** to drive the differential amplifier. At this time, the output is decided by the difference between the two inputs depending on a characteristic of the differential amplifier. In other words, a logical status of the fourteenth node **Q14** is changed by the different in the voltage between the first compare signal **VBDIV** inputted to the gate terminal of the twelfth NMOS transistor **N12** and the second compare signal **REFCRV** inputted to the gate terminal of the thirteenth NMOS transistor **N13**. For example, if the voltage of the tenth node **Q10** is lower than that of the eleventh node **Q11**, the fourteenth node **Q14** outputs a signal of a logical Low status. On the contrary, if the voltage of the tenth node **Q10** is higher than that of the eleventh node **Q11**, the fourteenth node **Q14** outputs a signal of a logical High status.

The clock control signal output unit **140** changes the logical status of the first and second clock control signals **PBIAS** and **NBIAS** output terminal

using the compare result signal being the output of the compare unit **120**. In other words, the compare result signal being the output of the compare unit **120** becomes the first clock control signal **PBIAS** and controls the fifteenth NMOS transistor **N15**. While the power supply voltage **VCC** having a logical status High by the nineteenth PMOS transistor **P19** is applied to the output terminal of the second clock control signal **NBIAS**, its value is changed depending on whether the fifteenth NMOS transistor **N15** operates. In concrete, if the compare result signal being the output of the fourteenth node **Q14** becomes a logical High, the fifteenth NMOS transistor **N15** is turned on and the logical status of the second clock control signal **NBIAS** is thus changed to a logical Low. Further, if the compare result signal being the output of the fourteenth node **Q14** become a logical Low, the fifteenth NMOS transistor **N15** is turned off and the logical status of the second clock control signal **NBIAS** is thus changed to a logical High.

As described above, the logical status of the first and second clock control signals are decided by the different between the first and second compare signals. This necessitates generation of the second compare signal of a constant level in order to control the boosting voltage. For this, the package voltage generating unit **150** controls the level of the second compare signal by controlling the channel width of the sixteenth PMOS transistor **P16** within the reference voltage generating unit using the package voltage signal **PVT**, which will be described by reference to FIG. 3.

FIG. 3A ~ FIG. 3C are circuit diagrams of the package voltage generating unit according to the present invention for explaining the

construction and operation of the unit.

Referring to FIG. 3A ~ FIG. 3C, the package voltage generating unit **150** comprises a trim bit input unit (see **152** in FIG. 3A), a voltage level converting unit (see **154** in FIG. 3B) and a package voltage output unit (see **156** in FIG. 3C). The trim bit input unit **152**, the voltage level converting unit **154** and the package voltage output unit **156** are serially connected. 'A', 'B', 'C', 'D', 'E' and 'F' in FIG. 3A sequentially correspond to 'A', 'B', 'C', 'D', 'E' and 'F' in FIG. 3B, respectively. 'G' in FIG. 3B corresponds to 'G' in FIG. 3C.

The trim bit input unit **152** outputs control signals of a plurality of levels depending on external trim bits to control the voltage level converting unit **154**. The voltage level converting unit **154** outputs voltages of various levels using the level control signal being the output of the trim bit input unit. The package voltage output unit **156** serves to prevent leakage of the output voltage of the voltage level converting unit **154** and outputs the package voltage signal **PVT** to the reference voltage generating unit **130**.

The package voltage generating unit of the present invention comprises the trim bit input unit **152**, the voltage level converting unit **154** and the package voltage output unit **156**. The trim bit input unit **152** comprises tenth ~ thirteenth inverters **I10** through **I13** and tenth ~ thirteenth NAND gates **ND10** through **ND13**. The voltage level converting unit **154** comprises thirtieth ~ sixtieth PMOS transistors **P30** through **P63**. The package voltage output unit **156** comprises thirtieth ~ thirty-fifth NMOS transistors **N30** through **N35**.

The trim bit input unit (FIG. 3A), the voltage level converting unit (FIG.

3B) and the package voltage output unit (FIG. 3C) will be below described in detail by reference to the accompanying drawings.

A first trim bit input terminal **TE1** is connected to a first input terminal of the tenth NAND gate **ND10** via the tenth inverter **I10** and is also connected
5 to a first input terminal of the twelfth NAND gate **ND12**. Further, the first trim bit input terminal **TE1** is connected to a second input terminal of the eleventh NAND gate **ND12** and a first input terminal of the thirteenth NAND gate **ND13**.

A second trim bit input terminal **TE2** is connected to the second input
10 terminal of the tenth NAND gate **ND10** via the eleventh inverter **I11** and is also connected to the first input terminal of the eleventh NAND gate **ND11**. Also, the second trim bit input terminal **TE2** is connected to the second input terminals of the twelfth and thirteenth NAND gates **ND12** and **ND13**.

A third trim bit input terminal **TE3** is connected to the gate terminal of
15 the fifty-third PMOS transistor **P53** via the twelfth inverter **I12**. Further, the third trim bit input terminal **TE3** is connected to the gate terminal of the thirty-third PMOS transistor **P33** via the twelfth and thirteenth inverters **I12** and **I13**.

The output terminal of the tenth NAND gate **ND10** is connected to the gate terminals of the thirtieth and thirty-eighth PMOS transistors **P30** and **P38**.
20 The output terminal of the eleventh NAND gate **ND11** is connected to the gate terminals of the thirty-first and forty-first PMOS transistors **P31** and **P41**. The output terminal of the twelfth NAND gate **ND12** is connected to the gate terminals of the thirty-second and forth-sixth PMOS transistors **P32** and **P46**. The output terminal of the thirteenth NAND gate **ND13** is connected to the

gate terminal of the fifth-fourth PMOS transistor **P54**.

The thirty-third PMOS transistor **P33** is connected between the power supply voltage **VCC** and the twentieth node **Q20**. The fifty-third PMOS transistor **P53** is connected between the power supply voltage **VCC** and the
5 twenty-fifth node **Q25**. The thirtieth PMOS transistor **P30** is connected between the twentieth node **Q20** and the twenty-third node **Q23**. The thirty-first PMOS transistor **P31** is connected between the twentieth node **Q20** and the twenty-second node **Q22**. The thirty-second PMOS transistor **P32** is connected between the twentieth node **Q20** and the twenty-first node **Q21**.

10 The thirty-fourth PMOS transistor **P34** is connected between the twentieth node **Q20** and the twenty-first node **Q21**. The thirty-fifth PMOS transistor **P35** is connected between the twenty-first node **Q21** and the twenty-second node **Q22**. The thirty-sixth PMOS transistor **P36** is connected between the twenty-second node **Q22** and the twenty-third node **Q23**. The
15 thirty-seventh PMOS transistor **P37** is connected between the twenty-third node **Q23** and the twenty-fourth node **Q24**. This means that the thirty-fourth ~ thirty-seventh PMOS transistors **P34** through **P37** are serially connected between the twentieth node **Q20** and the twenty-fourth node **Q24**. Further, the gate terminals of the thirty-fourth ~ thirty-seventh PMOS transistors **P34**
20 through **P37** are connected to the twenty-fourth node **Q24**, respectively.

The thirty-eighth ~ fortieth PMOS transistors **P38** through **P40** are serially connected between the twenty-fourth node **Q24** and the twenty-fifth node **Q25**. Each of the gate terminals of the thirty-ninth and fortieth PMOS transistors **P39** and **P40** are connected to the twenty-fourth node **Q24**.

The forty-first PMOS transistor **P41** is connected between the twenty-fifth and twenty-sixth nodes **Q25** and **Q26**. The forty-second and forty-third PMOS transistors **P42** and **P43** are serially connected between the twenty-fourth and twenty-sixth nodes **Q24** and **Q26**. The gate terminals of the forty-second and forty-third PMOS transistors **P42** and **P43** are driven by the twenty-fourth node **Q24**. Further, the forty-fourth and forty-fifth PMOS transistors **P44** and **P45** are serially connected between the twenty-second and twenty-sixth nodes **Q24** and **Q26**. The gate terminals of the forty-fourth and forty-fifth PMOS transistors **P44** and **P45** are driven by the twenty-fourth node **Q24**. In other words, the forty-second and forty-third PMOS transistors **P42** and **P43** and the forty-fourth and forty-fifth PMOS transistors **P44** and **P45**, which are serially connected, are connected in parallel between the twenty-fourth and twenty-sixth nodes **Q24** and **Q26**.

The forty-sixth PMOS transistor **P46** is connected between the twenty-fifth and twenty-seventh nodes **Q25** and **Q27**. Each of the forty-seventh and forty-eighth PMOS transistors **P47** and **P48**, the forty-ninth and fiftieth PMOS transistors **P49** and **P50**, and the fifty-first and fifty-second PMOS transistors **P51** and **P52** is serially connected between the twenty-fourth and twenty-seventh nodes **Q24** and **Q27**. Each of the forty-seventh ~ fifty-second PMOS transistors **P47** through **P52** is driven by the twenty-fourth node **Q24**. The forty-seventh and forty-eighth PMOS transistors **P47** and **P48**, the forty-ninth and fiftieth PMOS transistors **P49** and **P50**, and the fifty-first and fifth-second PMOS transistors **P51** and **P52**, each of which is serially connected, is connected in parallel between the twenty-four and twenty-seventh nodes **Q24**

and **Q27**.

The fifth-fourth PMOS transistor **P54** is connected between the twenty-fifth and twenty-eighth nodes **Q25** and **Q28**. Each of the fifth-fifth and fifth-sixth PMOS transistors **P55** and **P56**, the fifth-seventh and fifth-eighth PMOS transistors **P57** and **P58**, the fifty-ninth and sixtieth PMOS transistors **P59** and **P60**) and the sixty-first and sixth-second PMOS transistors **P61** and **P62** is serially connected between the twenty-fourth and twenty-eighth nodes **Q24** and **Q28**. Each of the fifth-fifth ~ sixty-second PMOS transistors **P55** through **P62** is driven by the twenty-fourth node **Q24**. The fifty-fifth and
10 fifty-sixth PMOS transistors **P55** and **P56**, the fifty-seventh and fifty-eighth PMOS transistors **P57** and **P58**, the fifty-ninth and sixtieth PMOS transistors **P59** and **P60**, and the sixty-first and sixty-second PMOS transistors **P61** and **P62**, each of which is serially connected, is connected in parallel between the twenty-fourth and twenty-eighth nodes **Q24** and **Q28**. The sixty-third PMOS
15 transistor **P63** is connected between the twenty-second **Q24** and the twenty-fifth node **Q25**. The gate terminal is connected to the twenty-fourth node **Q24**.

The thirtieth ~ thirty-fifth NMOS transistors **N30** through **N35** are serially connected between the twenty-fourth node ('G' in FIG. 3B and FIG.
20 3C, **Q24**) and the ground **VSS**. Each of the gate terminals of the thirtieth ~ thirty-fifth NMOS transistors **N30** through **N35** are connected to the ground **VSS**.

The operation of the package voltage generating unit **150** constructed above, for using the external trim bits to output the package voltages of

various levels, will be below described.

A first trim bit signal **STE1** of the first trim bit input terminal **TE1** is applied to the input terminals of the eleventh and thirteenth NAND gates **ND11** and **ND13**. Next, the first trim bit signal **STE1** is inverted by the tenth inverter **I10** and is then applied to the input terminals of the tenth and twelfth NAND gates **ND10** and **ND12**.

A second trim bit signal **STE2** of the second trim bit input terminal **TE2** is applied to the input terminals of the twelfth and thirteenth NAND gates **ND12** and **ND13**. Next, the second trim bit signal **STE2** is inverted by the eleventh inverter **I11** and is then applied to the input terminals of the tenth and eleventh NAND gates **ND10** and **ND11**.

The tenth NAND gate **ND10** logically combines the first and second trim bit signals **STE1** and **STE2**, which were inverted, and then outputs a first voltage level control signal **VLC1** to the gate terminal of the thirtieth and thirty-eighth PMOS transistors **P30** and **P38**. The eleventh NAND gate **ND11** logically combines the second trim bit signal **STE2** and the first trim bit signal **STE1**, which were inverted, and then outputs a second voltage level control signal **VLC2** to the gate terminal of the thirty-first and forty-first PMOS transistors **P31** and **P41**. The twelfth NAND gate **ND12** logically combines the first trim bit signal **STE1** and the second trim bit signal **STE2**, which were inverted, and then outputs a third voltage level control signal **VLC3** to the gate terminal of the thirty-second and forty-sixth PMOS transistors **P32** and **P46**. The thirteenth NAND gate **ND13** logically combines the first and second trim bit signals **STE1** and **STE2** and then output

a fourth voltage level control signal **VLC4** to the gate terminal of the forty-fourth PMOS transistor **P54**.

For example, if both logical status of the first and second trim bit signals **STE1** and **STE2** are Low, the tenth NAND gate **ND10** outputs the first
5 voltage level control signal **VLC1** having a Low status, and the eleventh ~
thirteenth NAND gates **ND11** through **N13** outputs the second ~ fourth voltage
level control signals **VLC2** through **VLC4** having a High status, respectively.
Further, if the logical status of the first and second trim bit signals **STE1** and
STE2 are High and Low, respectively, the eleventh NAND gate **ND11** outputs
10 the second voltage level control signal **VLC2** having a Low status. Also, if a
logical status of each of the first and second trim bit signals **STE1** and **STE2** is
Low and High, the twelfth NAND gate **ND12** outputs the third voltage level
control signal **VLC3** having a Low status. If a logical status of the first and
second trim bit signals **STE1** and **STE2** is all Low, the thirteenth NAND gate
15 **ND13** outputs he fourth voltage level control signal **VLC4** having a Low
status.

The third trim bit signal **STE3** in the third trim bit input terminal **TE3** is
inverted by the twelfth inverter **I12** (first path control signal; **RTE**) and then
applied to the fifty-third PMOS transistor **P53**. Further, the third trim bit
20 signal **STE3** inverted by the twelfth inverter **I12** is inverted by the thirteenth
inverter **I13** (second path control signal; **IRTE**) and then applied to the thirty-
third PMOS transistor **P33**. The path of the power supply voltage **VCC** is
adjusted by controlling the thirty-third and the fifty-third PMOS transistors
P33 and **P53** within the voltage level converting unit **154** by means of the third

trim bit signal **STE3**.

In more detail, if the third trim bit signal **STE3** of a logical High is inputted, the first path control signal **RTE** of an inverted Low status is outputted by the twelfth inverter **I12**, and the second path control signal **IRTE** of a logical High is outputted by the thirteenth inverter **I13**. Accordingly, the fifth-third PMOS transistor **P53** is driven by the first path control signal **RTE** and the power supply voltage **VCC** is thus applied to the twenty-fifth node **Q25**. If the third trim bit signal **TE3** of a logical Low is inputted, the first path control signal **RTE** of a logical High is outputted by the twelfth inverter **I12**, and the second path control signal **IRTE** of a logical Low is outputted by the thirteenth inverter **I13**. Accordingly, the thirty-third PMOS transistor **P33** is driven by the second path control signal **IRTE** and the power supply voltage **VCC** is thus applied to the twentieth node **Q20**.

By means of the first ~ fourth voltage level control signals **VLC1** through **VLC4** and the first and second path control signals **RTE** and **IRTE**, the voltage level converting unit **154** outputs package voltage signals of first ~ seventh voltage levels.

A case that the fifty-third PMOS transistor **P53** is turned off by the second path control signal **IRTE** and the thirty-third PMOS transistor **P33** is turned on,, will be first examined. The voltages of the first ~ third voltage levels are applied to the output terminals by means of the first ~ third voltage level control signals **VLC1** through **VLC3**.

In concrete, the thirtieth PMOS transistor **P30** is turned on by the first voltage level control signal **VLC1**. A voltage is dropped and divided by the

thirty-third, the thirtieth and the thirty-seventh PMOS transistors **P33**, **P30** and **P37**, and a voltage of the first voltage level is thus applied to the output terminal. The thirty-first PMOS transistor **P31** is turned on by the second voltage level control signal **VLC2**. A voltage is dropped and divided by the
5 thirty-third and the thirty-first PMOS transistors **P33** and **P31** and the thirty-sixth and the thirty-seventh PMOS transistors **P36** and **P37**, and a voltage of the second voltage level is thus applied to the output terminal. The thirty-second PMOS transistor **P32** is turned on by the third voltage level control signal **VLC3**. A voltage is dropped and divided by the thirty-third and thirty-second PMOS transistors **P33** and **P32** and the thirty-fifth and thirty-seventh
10 PMOS transistors **P35** through **P37**, and a voltage of the third voltage level is thus applied to the output terminal.

A case that the thirty-third PMOS transistor **P33** is turned off by the first path control signal **RTE** and the fifty-third PMOS transistor **P53** is turned off,
15 will be first examined. The voltages of the fourth ~ seventh voltage levels are applied to the output terminals by means of the first ~ fourth voltage level control signals **VLC1** through **VLC4**.

In concrete, the thirty-eighth PMOS transistor **P38** is turned on by the first voltage level control signal **VLC1**. A voltage is dropped and divided by
20 the fifth-third and thirty-eighth PMOS transistors **P53** and **P38**, the thirty-ninth and fortieth PMOS transistors **P39** and **P40**, and the sixty-third PMOS transistor **P63**, and a voltage of the fourth voltage level is thus applied to the output terminal. The forty-first PMOS transistor **P41** is turned on by the second voltage level control signal **VLC2**. A voltage is dropped and divided

by the fifty-third and forty-first PMOS transistors **P53** and **P41**, the forty-second and forty-third PMOS transistors **P42** and **P43**, the forty-fourth and forty-fifth PMOS transistors **P44** and **P45**, and the sixty-third PMOS transistor **P63**, and a voltage of the fifth voltage level is thus applied to the output terminal. The forty-sixth PMOS transistor **P46** is turned on by the third voltage level control signal **VLC3**. A voltage is dropped and divided by the fifty-third and forty-third PMOS transistors **P53** and **P46**, the forty-seventh and forty-eighth PMOS transistors **P47** and **P48**, the forty-ninth and fiftieth PMOS transistors **P49** and **P50**, the fifty-first and fifty-second PMOS transistors **P51** and **P52**, and the sixty-third PMOS transistor **P63**, and a voltage of the sixth voltage level is applied to the output terminal. The fifty-fourth PMOS transistor **P54** is turned on by the fourth voltage level control signal **VLC4**. A voltage is dropped and divided by the fifty-third and fifty-fourth PMOS transistors **P53** and **P54**, the fifty-fifth and fifty-sixth PMOS transistors **P55** and **P56**, the fifty-seventh and fifty-eighth PMOS transistors **P57** and **P58**, the fifty-ninth and sixtieth PMOS transistors **P59** and **P60**, the sixty-first and sixty-second PMOS transistors **P61** and **P62**, and the sixty-third PMOS transistor **P63**, and a voltage of the seventh voltage level is thus applied to the output terminal. In other words, the number of the PMOS transistors connected in parallel depending on the turned-on status of the thirty-eighth, forty-first, forty-sixth and fifty-fourth PMOS transistors **P38**, **P41**, **P46** and **P54**. Thereby, voltages and currents of various levels are outputted.

The output unit **156** has a leakage current using the thirtieth ~ thirty-third NMOS transistors **N30** through **N35** and outputs the first ~ seventh

voltage level signals **PVT** being the output of the voltage level converting unit **154** to the compare reference voltage generating means **130**.

The second compare reference signal **REFCRV** and the control signal **NGATE**, being the outputs of the reference voltage generating unit **130**, are
5 changed by the package voltage **PVT** (first ~ seventh voltage levels) outputted from the package voltage generating unit **150** having the above construction and operation. It is thus possible to variably set the reference voltage (second compare reference signal **REFCRV**) for controlling the boosting voltage to be a given level.

10 As described above, the regulation block **100** compares the reference voltage internally generated and the inputted boosting voltage. The regulating block **100** then changes the logical status of the first and second clock control signals **PBIAS** and **NBIAS** for controlling the clock generator **200**, depending on whether the level of the inputted boosting voltage is higher
15 or lower than that of the reference voltage. As such, the regulation block **100** controls the clock generator **200** to control the level of the boosting voltage.

The clock generator **200** controlled by the first and second clock control signals **PBIAS** and **NBIAS** from the regulation block **100** will be described.

FIG. 4 is a circuit diagram of the clock generator according to the
20 present invention for explaining the construction and operation of the generator.

Referring to FIG. 4, the clock generator **200** comprises first ~ fifth clock generating units **210** through **250**. Each of the first ~ fifth clock generating units **210** through **250** is connected to the external first and second clock

control signals **PBIAS** and **NBIAS**. The output terminals of the first ~ fifth clock generating units **210** through **250** are connected to the input terminals of their front stages, thus forming a loop.

The first ~ fifth clock generating units **210** through **250** have the same construction. Therefore, only the first clock generating unit **210** will be
5 explained in order to avoid redundancy.

The first clock generating unit **210** has a first PMOS transistor **P1** driven by the external first clock control signal **PBIAS** and a second PMOS transistor **P2** driven by a fifth clock output terminal **CLK4**, which are serially
10 connected between the power supply voltage **VCC** and a first clock signal **CLK0** output terminal. The first clock generation unit **210** further comprises a first NMOS transistor **N1** driven by the second clock control signal **NBIAS** and a second NMOS transistor **N2** driven by the fifth clock output terminal **CLK4**, which are serially connected between the first clock signal **CLK0**
15 output terminal and the ground **VSS**.

In other words, the first PMOS transistor **P1**, the second PMOS transistor **P2**, the second NMOS transistor **N2** and the first NMOS transistor **N1** are sequentially serially connected between the power supply voltage **VCC** and the ground **VSS**. At this time, the first PMOS transistor **P1** and the first
20 NMOS transistor **N1** are each driven by the first and second clock control signals **PBIAS** and **NBIAS**. Also, the second PMOS transistor **P2** and the second NMOS transistor **N2** are driven by the output signal of the fifth clock signal **CLK4** output terminal being the output of the fifth clock generating unit **250**.

The operation of the above clock generator will be now described.

The first PMOS transistor **P1** is turned on or off by the first clock control signal **PBIAS** to control application of the power supply voltage **VCC** of a logical High status to the drain terminal of the second PMOS transistor **P2**.

5 Further, the first NMOS transistor **N1** is turned on or off by the second clock control signal **NBIAS** to control application of the ground **VSS** of a logical Low status to the drain terminal of the second NMOS transistor **N2**.

At this time, either the second PMOS transistor **P2** or the second NMOS transistor **N2** is turned by the logical status of the fifth clock signal **CLK4** being the output of the fifth clock generating unit **250**, thus outputting the first clock signal **CLK0** having an opposite logical status to the fifth clock signal **CLK4** to the output terminal of the first clock generating unit **210**. In other words, the first ~ fifth clock generating units **210** through **250** output logical signals having opposite logical status to the output signal of the front stage.

15 In concrete, when the initial logical status of the first ~ fifth clock signals **CLK0** through **CLK4** are High, Low, High, Low and High, and the first and second clock control signals **PBIAS** and **NBIAS** are applied with Low and High, will be examined as follows.

As described above, the first PMOS and first NMOS transistors **P1** and **N1** in the first clock generating unit **210** are turned on by the first and second clock control signals **PBIAS** and **NBIAS**. Further, the second NMOS transistor **N2** is turned on by the fifth clock signal **CLK4** of a logical High status. Thereby, the first clock generating unit **210** receives the fifth clock signal **CLK4** of the logical High status to output the first clock signal **CLK0**

of a logical Low status. The second clock generating unit **220** receives the first clock signal **CLK0** of the logical Low status to output the second clock signal **CLK1** of a logical High status. The third clock generating unit **230** receives the second clock signal **CLK1** of the logical High status to output the third clock signal **CLK2** of a logical Low status. The fourth clock generating unit **240** receives the third clock signal **CLK2** of the logical Low status to output the fourth clock signal **CLK3** of a logical High status. The fifth clock generating unit **250** receives the fourth clock signal **CLK3** of the logical High status to output the fifth clock signal **CLK4** of a logical Low status. The first clock generating unit **210** receives the fifth clock signal **CLK4** of the logical Low status to output the first clock signal **CLK0** of a logical High status.

Examining the logical status of the first clock signal **CLK0**, it could be understood that the logical status is continuously changed from High to Low and vice versa. The first ~ fifth clock generating units **210** through **250** output the first ~ fifth clock signals **CLK0** through **CLK4** of a given frequency to control the first and second pumps **300** and **310**.

At this time, if a signal of a logical High status is inputted to the first clock control signal **PBIAS** or a signal of a logical Low status is inputted to the second clock control signal **NBIAS**, the first PMOS transistor **P1** is turned off or the second NMOS transistor **N2** is turned off. Thereby, as the clock signals of the first ~ fifth clock generating units **210** through **250** constantly keep a given logical status, it is possible to control the clock cycle.

As described above, according to the present invention, a trim bit is used to control the level of the **PVT** voltage and to control the compare

reference voltage generating unit. Further, the boosting voltage is controlled by comparing the dropped boosting voltage and the reference voltage of the compare reference voltage generating unit. Therefore, the present invention has an advantageous effect that it can stably control the boosting voltage with
5 a low power.

Further, a stable boosting voltage could be kept normally. Therefore, the present invention has a new effect that it can improve the speed of the read operation of the device.

The forgoing embodiments are merely exemplary and are not to be
10 construed as limiting the present invention. The present teachings can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art.